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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,029	02/25/2004	Daniel Boyko	A0312.70513US00	3915

7590 09/08/2005

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,029	BOYKO ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,8,10,17 and 18* is/are rejected.

7)☒ Claim(s) *6,7,9 and 11-16* is/are objected to.

8)☒ Claim(s) *19-25* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 recites the limitation "the clock generation circuit" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-5, 8, 10, and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Chiu et al. (U.S. Patent No. 6,687,320).

In reference to claim 1, Chiu discloses in Figure 1-2 a device having a clock generation circuit (150) which produces a first clock signal (CPU_CLK) for use in timing a) internal circuitry (110, 120) clocked by a first clock signal; b) at least one interface circuit (14N) clocked by a second clock (SYS_CLK) that interfaces to external circuitry, c) the clock generation circuit comprising: i) a phase locked loop (200) having an output,

ii) a first programmable frequency scaling circuit (26N, 270) having an input coupled to the output of the phase locked loop (200), an output of the first programmable frequency scaling circuit (26N, 270) providing the first clock signal (CLK1/CPU_CLK); and iii) a second programmable frequency scaling circuit (26N, 280) having an input coupled to the output of the phase locked loop (200), an output of the second programmable frequency scaling circuit (26N, 280) supplying the second clock signal (CLK2/SYS_CLK). The same applies to claim 10.

In reference to claim 3, Chiu discloses in Figure 2 that the first and second programmable frequency scaling circuits are programmable dividers.

In reference to claim 4, it is considered well known to one skilled in the art that dividers may be implemented using counters, of which fact official notice is taken. The same applies to claim 23.

In reference to claim 5, Chiu does not physically show the control logic, however he shows the multiplexers 270, 280 (which are considered to be part of the divider circuit) receiving selection signals. Therefore, there must be some type of control logic providing the control for these circuits. The same applies to claim 18.

In reference to claim 8, Chiu discloses in Figure 2 that the phase locked loop (240) additionally comprises a third programmable divider (23N, 240).

In reference to claim 17, Chiu discloses in Figure 2 that the frequency of the first clock (CLK1) and the second clock (CLK2) are able to be selected and can be chosen so that they are not integer multiples of each other (this is considered a design expedient based on the desired operation and outcome).

Allowable Subject Matter

5. Claims 19-25 are allowed.

6. Claims 6-7, 9, and 11-16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Claims 6-7 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the control logic (350) controls loading of a first programmable divider (340) when the control logic (350) detects an end of a period of the first clock (CCLK) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 9 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the device additionally comprises a control register (330) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 11 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the method includes changing the frequency of the first clock on the fly in combination with the rest of the limitations of the base claims and any intervening claims. Claims 12-16 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the method includes placing the chip in a first power saving mode by changing the first frequency ratio such that the first circuitry is clocked at a lower rate in combination with the rest of the limitations of the base claims and any intervening claims.

8. The following is an examiner's statement of reasons for allowance: Claims 19-25 are allowed because the closest prior art of record fails to disclose a circuit wherein the method includes waiting until a defined time relative to the period of the second clock (SCLK) while holding the state of the first clock; and loading the new value in a control location at the defined time in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

cc

September 2, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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